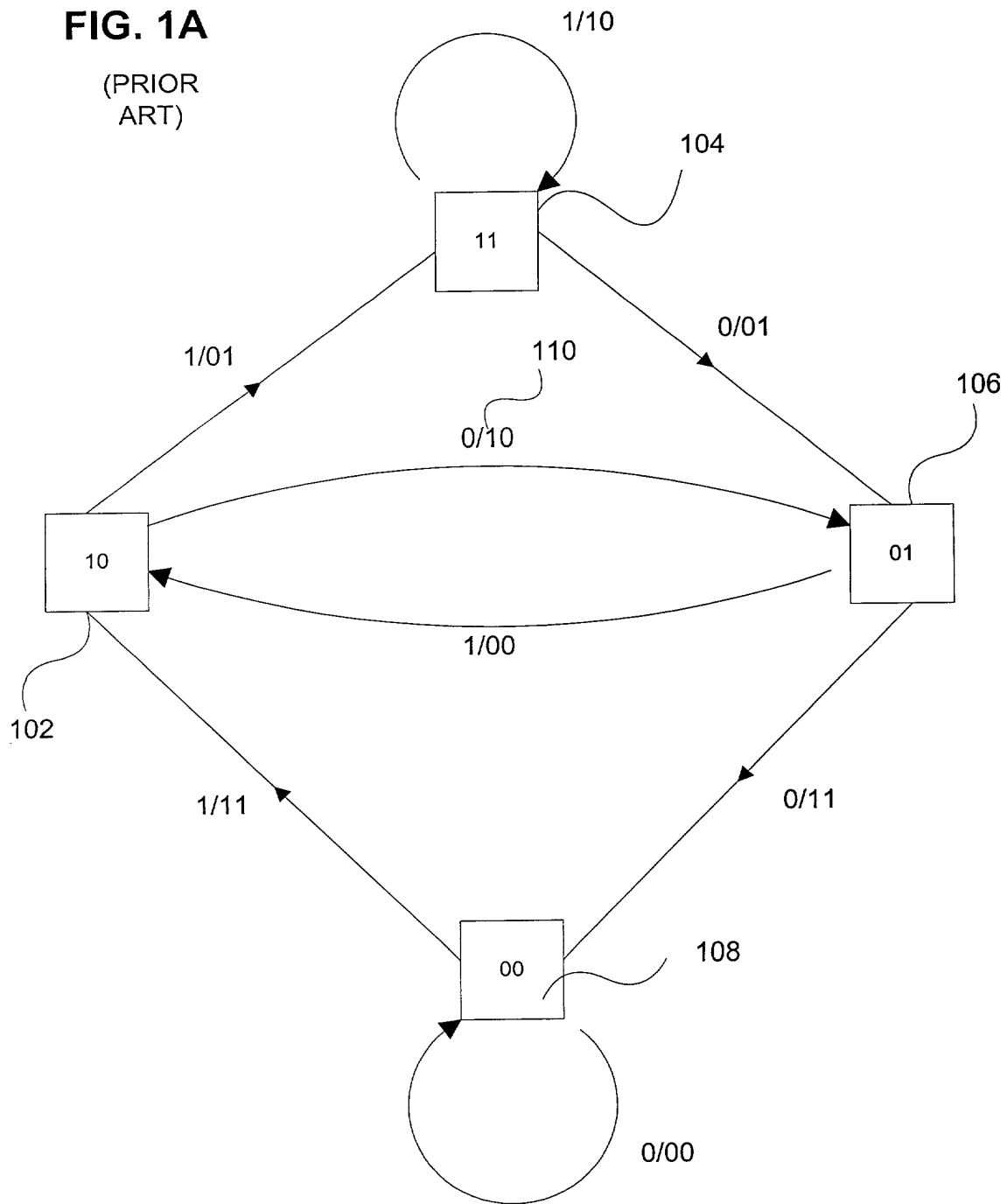


**FIG. 1A**

(PRIOR  
ART)



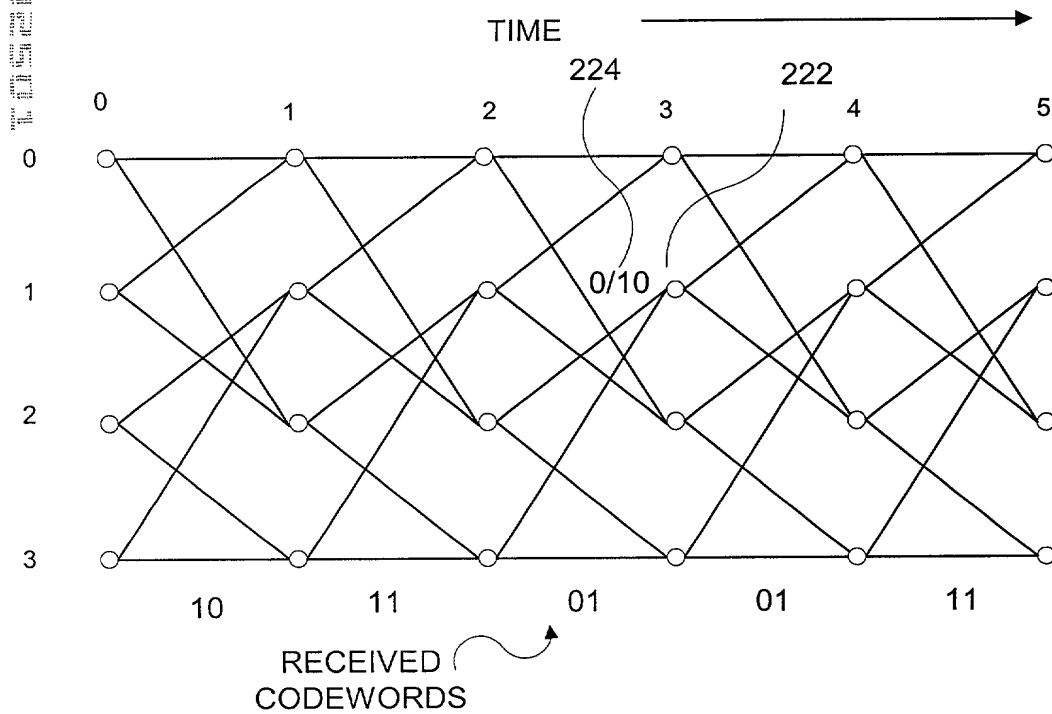
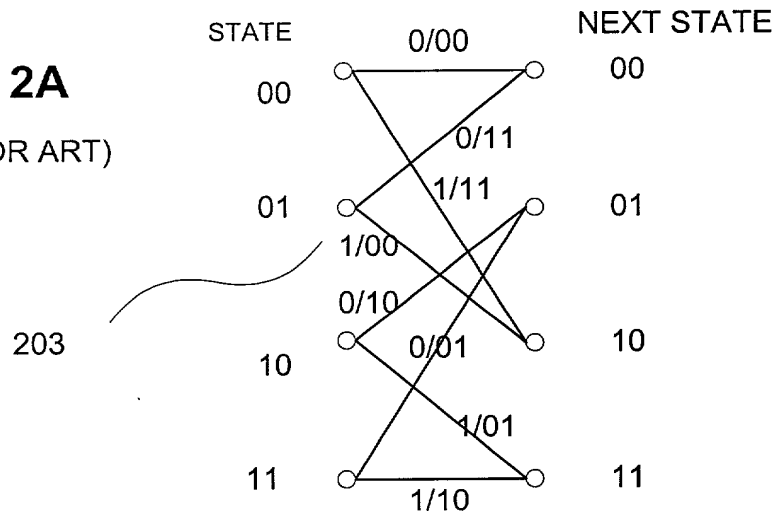
INPUT BIT	INITIAL STATE	NEXT STATE	OUTPUT CODEWORD
0	00	00	00
1	00	10	11
0	01	00	11
1	01	10	00
0	10	01	10
1	10	11	01
0	11	01	01
1	11	11	10

**FIG. 1B** (PRIOR ART)

FIG. 1B (PRIOR ART)

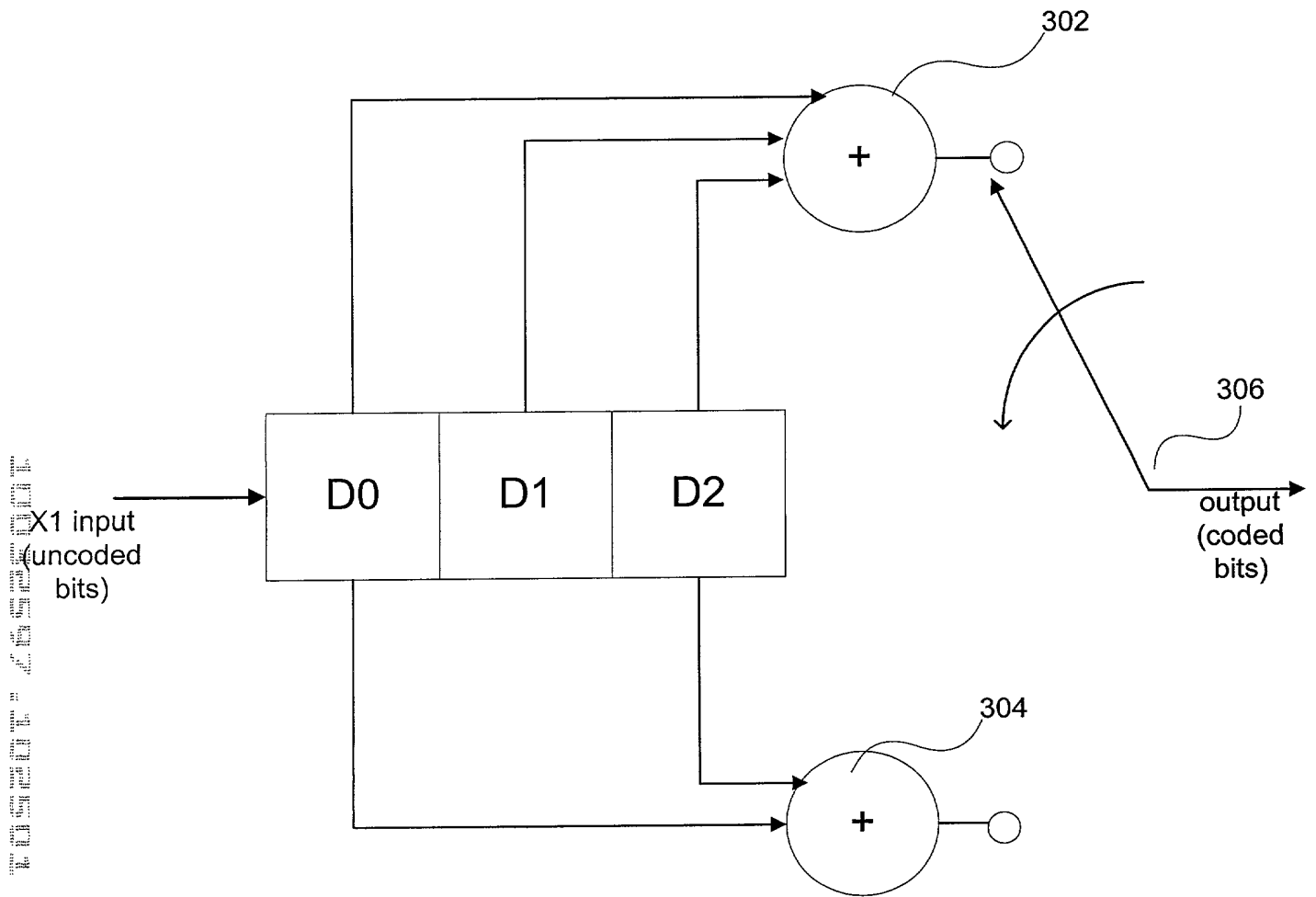
**FIG. 2A**

(PRIOR ART)



**FIG. 2B**

(PRIOR ART)



**FIG. 3** (Prior Art)

FIG. 4A

L=4

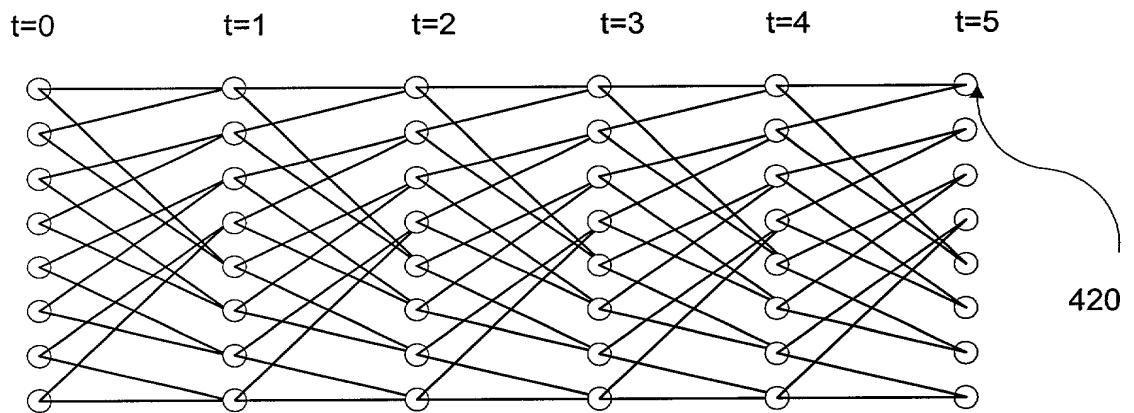
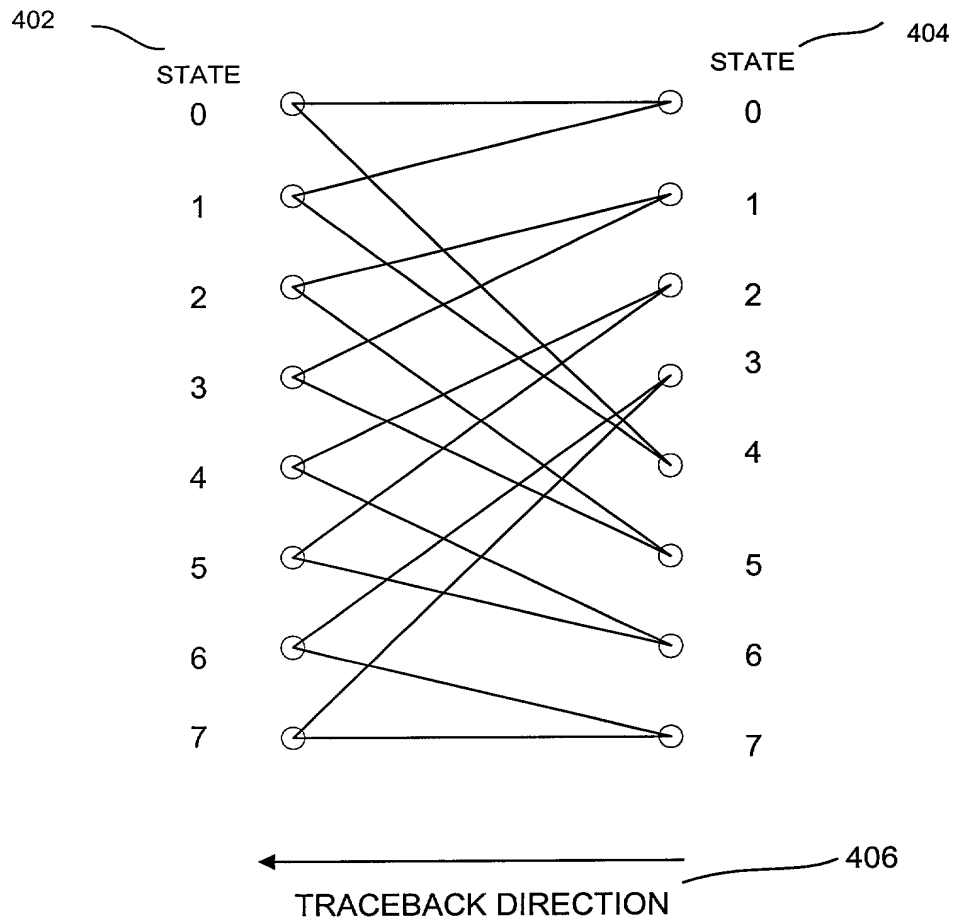


FIG. 4B

TRACEBACK LENGTH =  $v = 5$

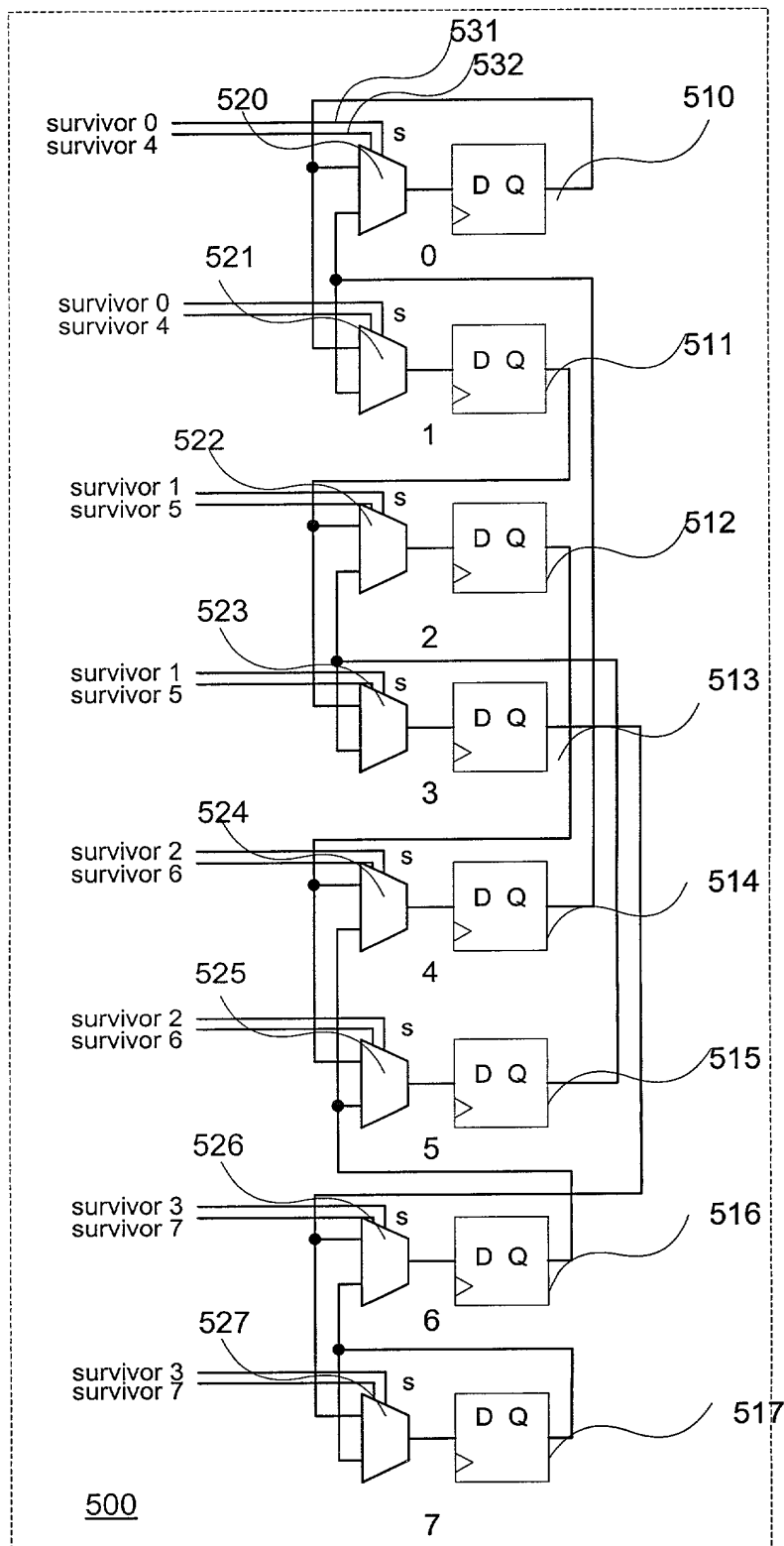
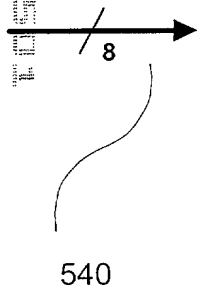


FIG. 5

FIG. 5A

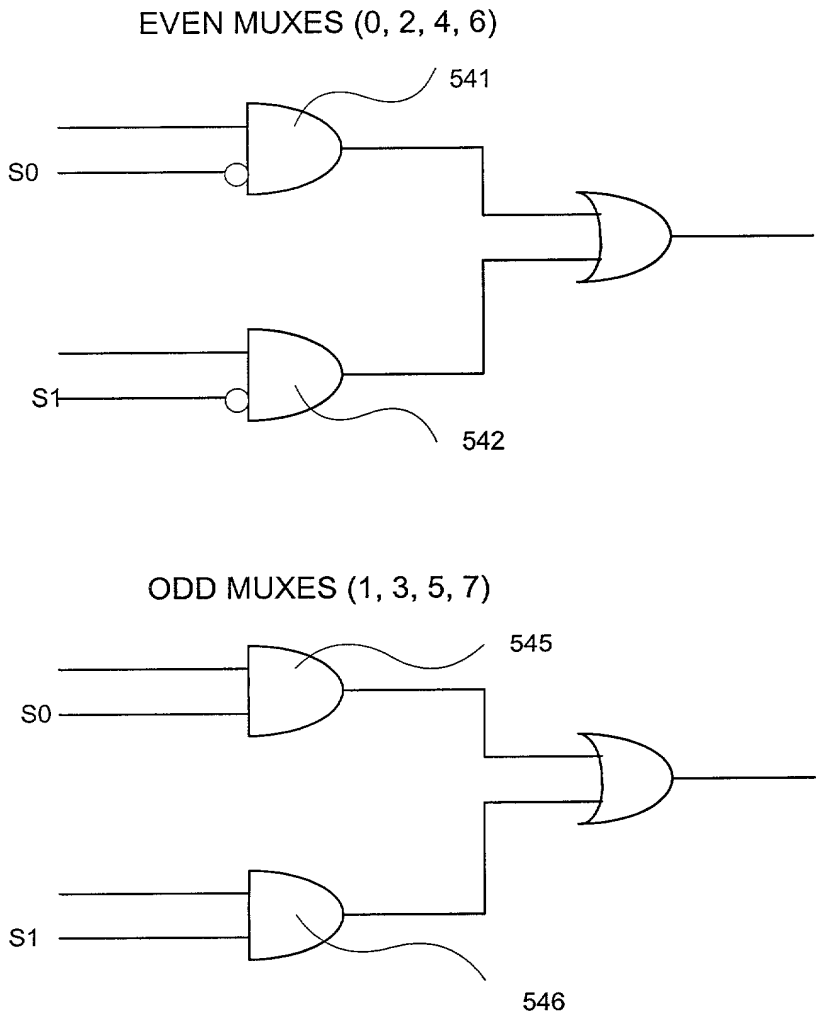
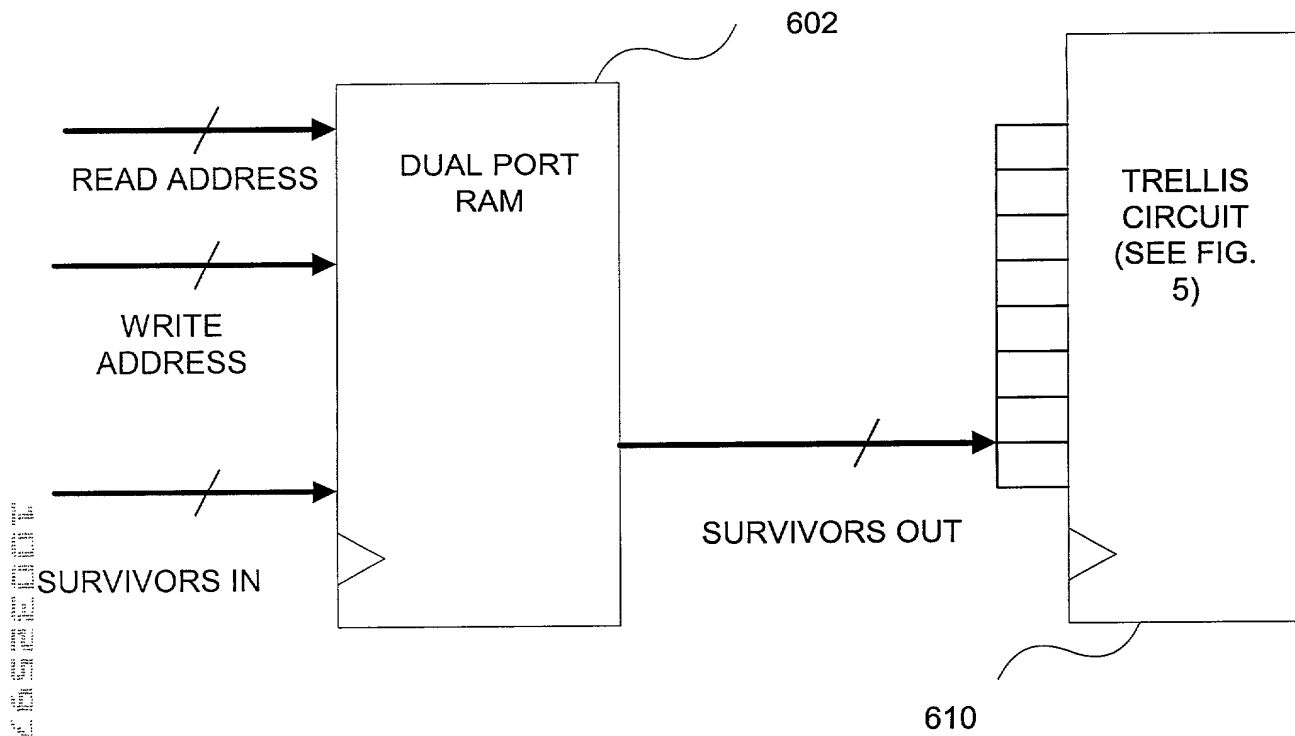
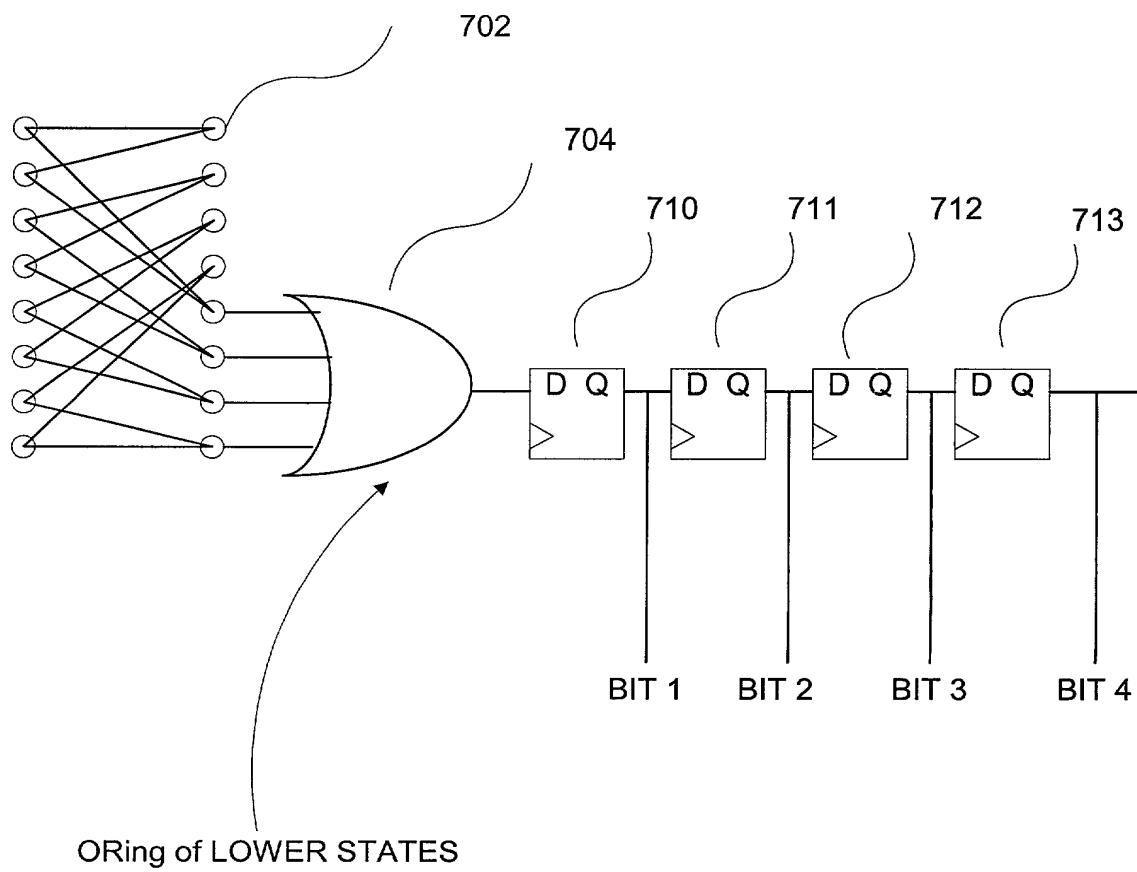


FIG. 5A

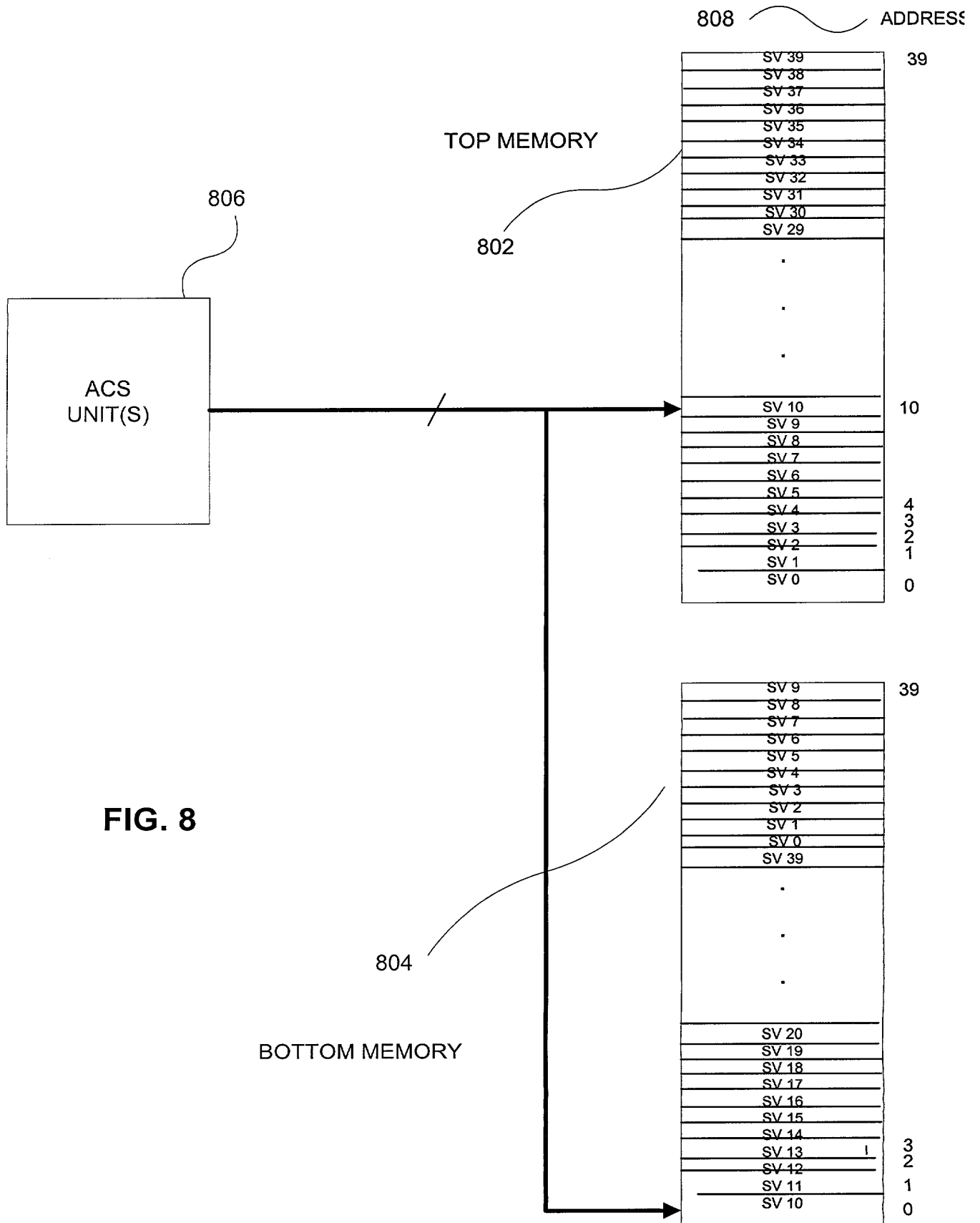


**FIG. 6**





**FIG. 7**



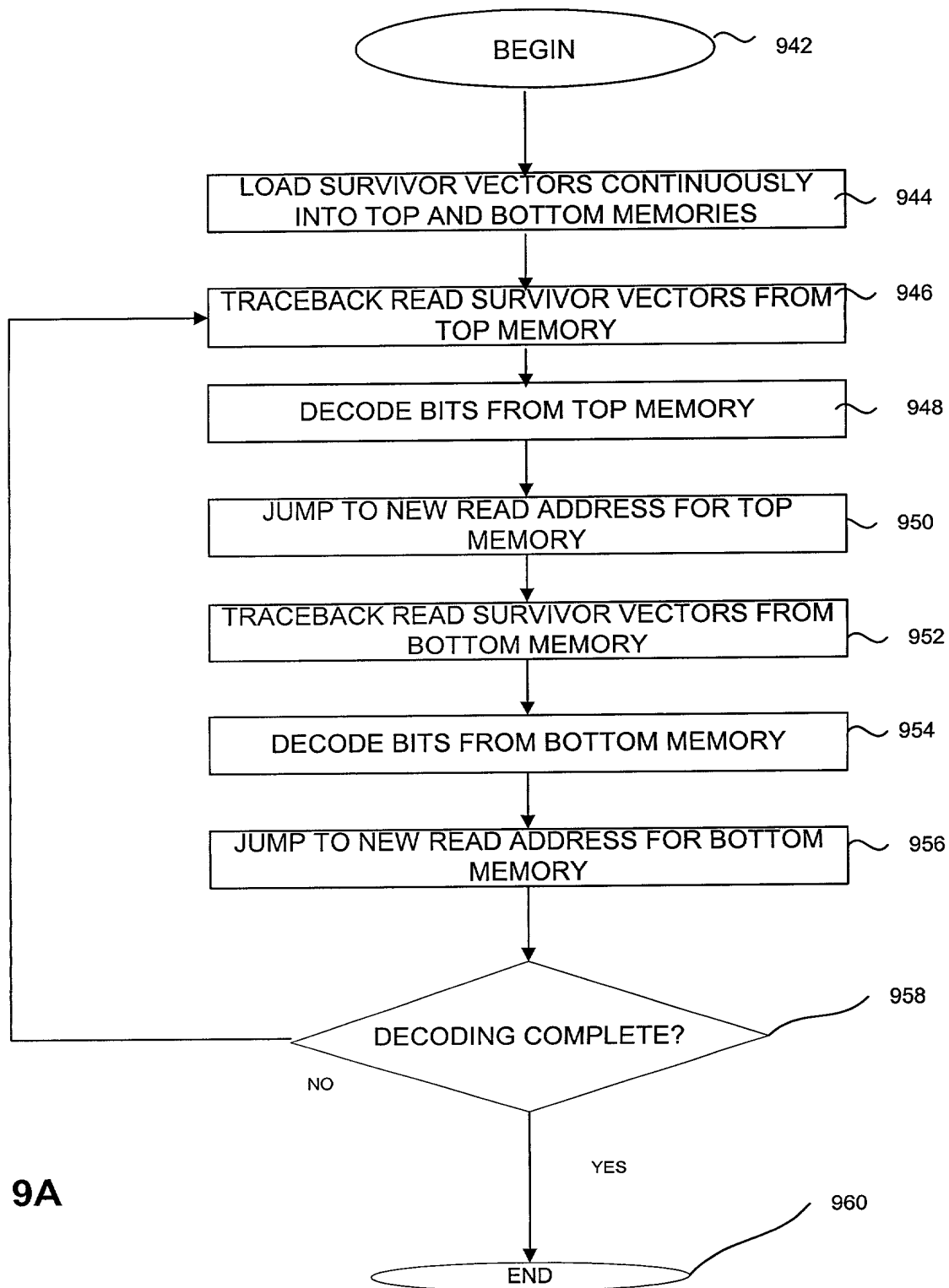
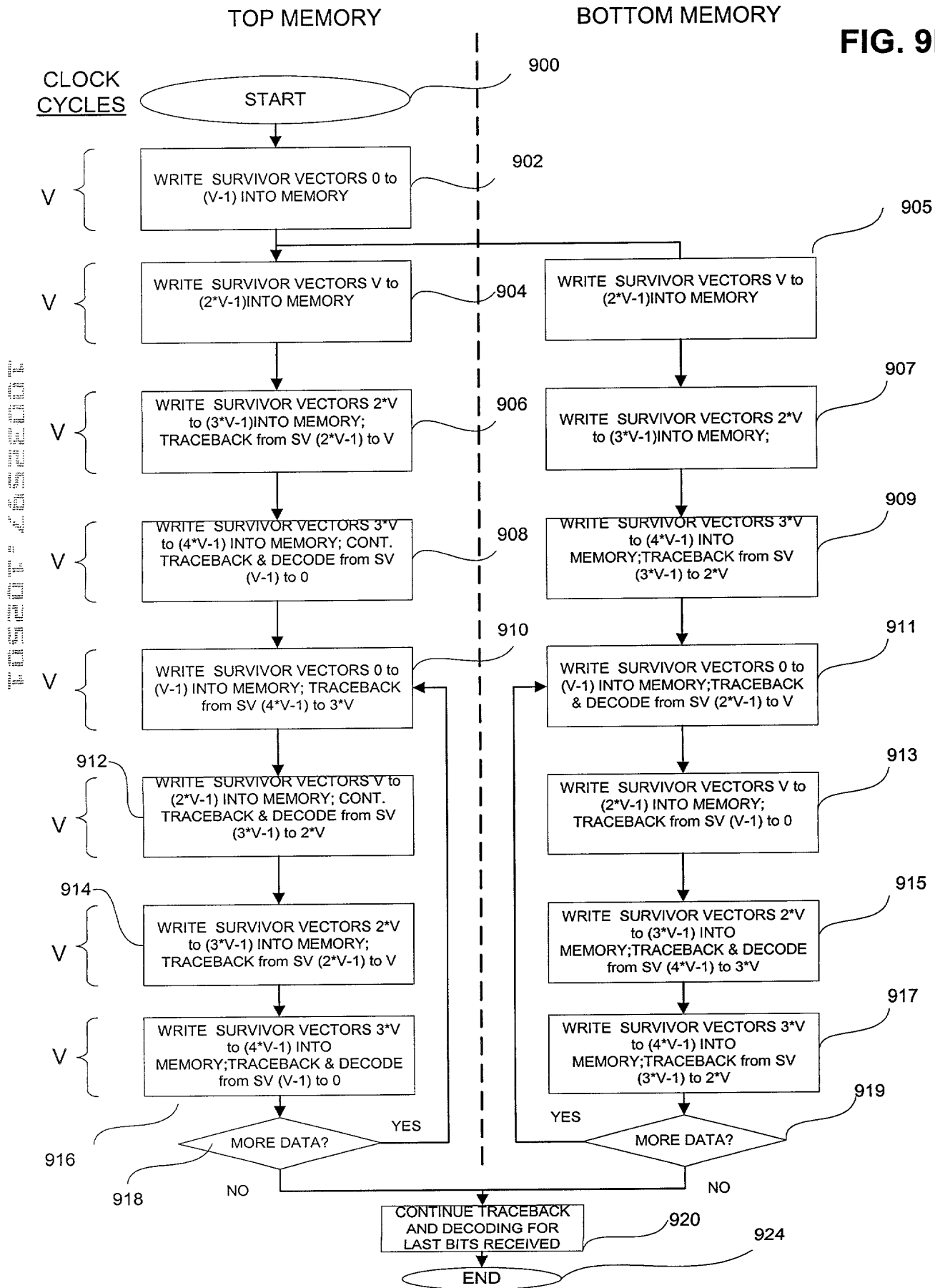
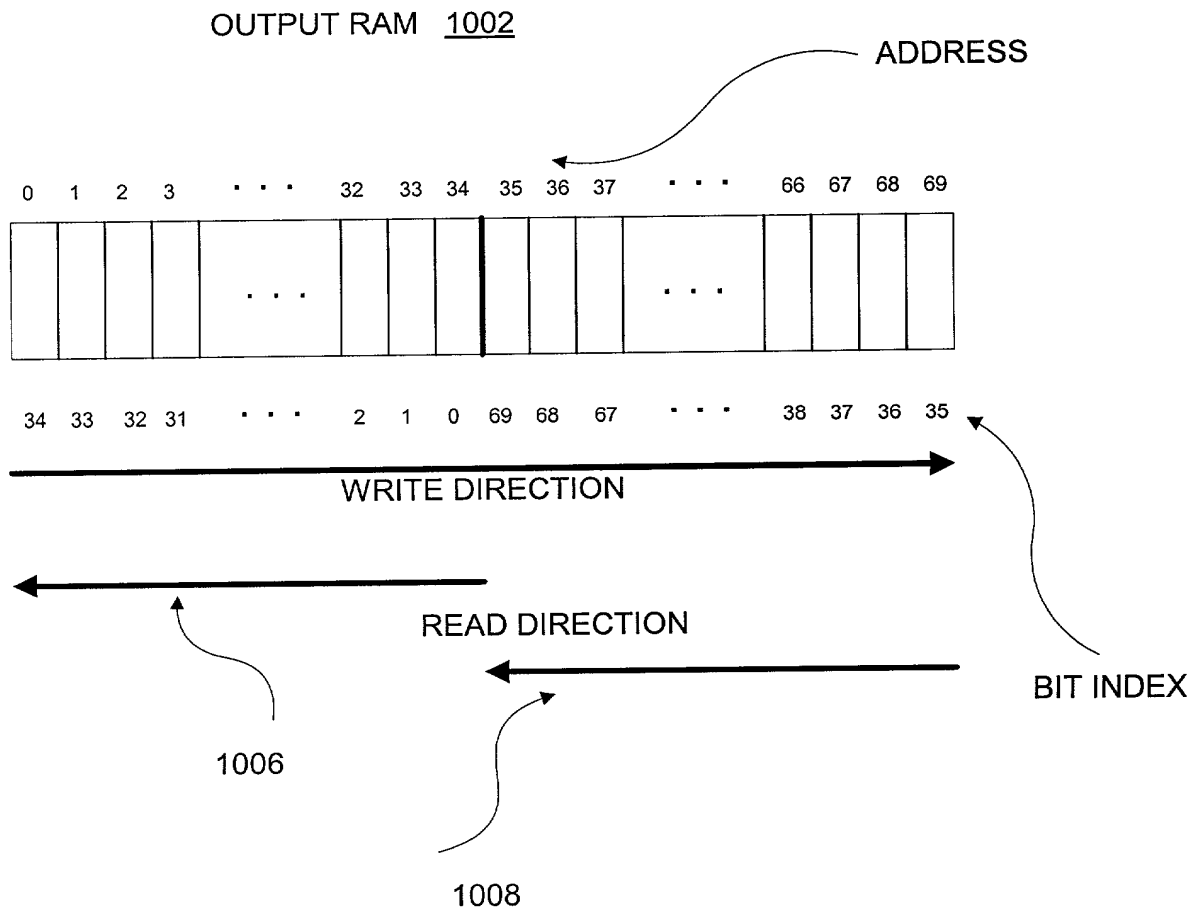


FIG. 9A

**FIG. 9B**





**FIG. 10**